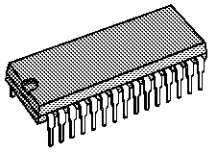
SGS-THOMSON MICROELECTRONICS

TDA7317

FIVE BANDS DIGITAL CONTROLLED GRAPHIC EQUALIZER

ADVANCE DATA

- VOLUME CONTROL IN 0.375dB STEP
- FIVE BANDS STEREO GRAPHIC EQUALIZER
- CENTER FREQUENCY, BANDWIDTH, MAX BOOST/CUT DEFINED BY EXTERNAL COMPONENTS
- ±14dB CUT/BOOST CONTROL IN 2dB/STEP
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS
- VERY LOW DISTORTION
- VERY LOW NOISE AND DC STEPPING BY USE OF A MIXED BIPOLAR/CMOS TECHNOLOGY



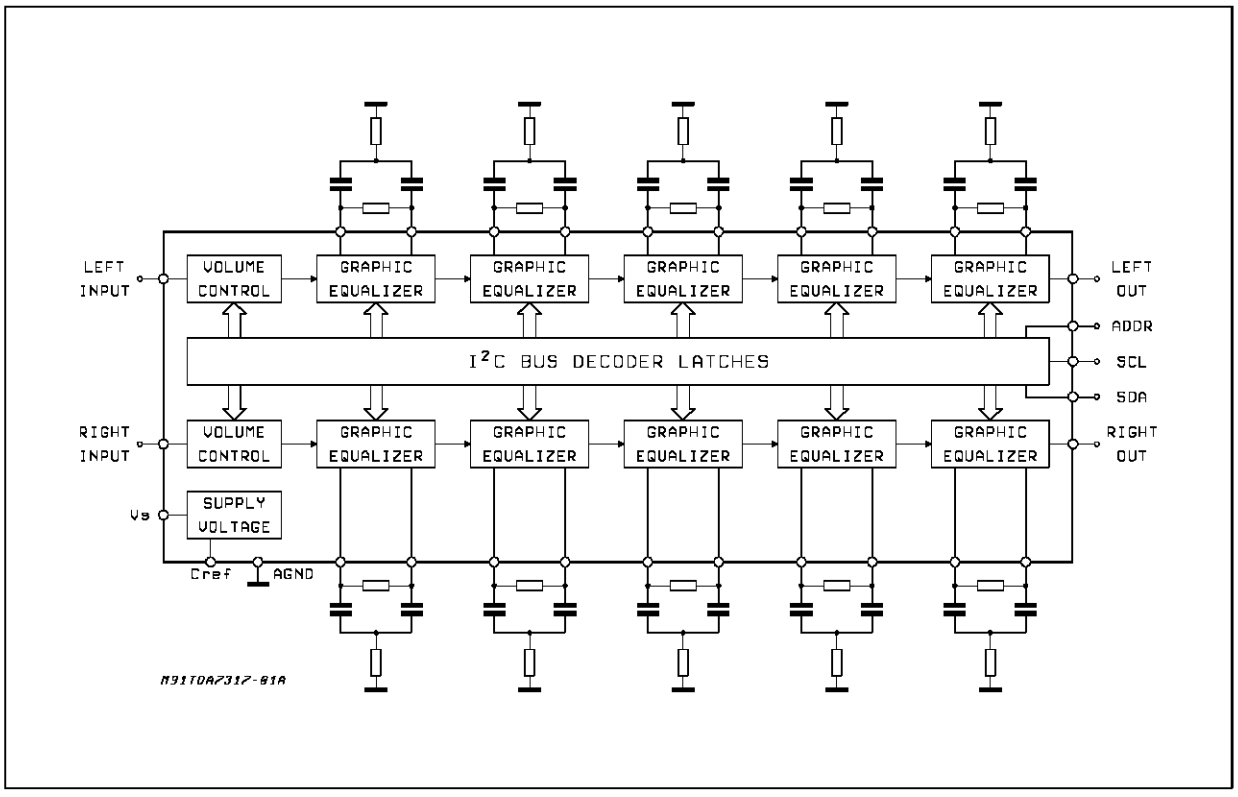
SDIP30

ORDERING NUMBER: TDA7317

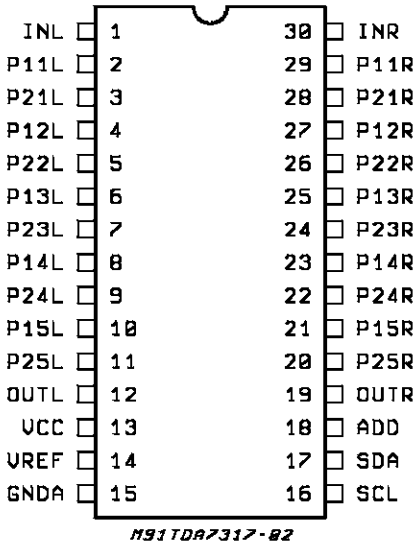
DESCRIPTION

The TDA7317 is a monolithic, digitally controlled graphic equalizer realized in BiCMOS mixed technology. The stereo signal, before any filtering, can be attenuated up to -17.625dB in 0.375dB step.
All the functions can be programmed via serial bus making easy to build a µP controlled system. Signal path is designed for very low noise and distortion.

BLOCK DIAGRAM



PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_S	Supply Voltage		10.2	V
T_{op}	Operating Temperature Range		-40 to +85	°C
T_{stg}	Storage Temperature Range		-55 to +150	°C
R_{tjvins}	Thermal Resistance Junction pins	max	85	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 9V, R_L = 10KΩ, R_g = 600Ω, f = 1KHz V_{IN} = 1Vrms, all controls in flat position (AV = 0dB) unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		6	9	10	V
I_S	Supply Current		8	14	20	mA
SVR	Ripple Rejection	f = 300Hz to 10KHz	60	80		dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INPUT						
R_I	Input Resistance		20	30	40	KΩ
$V_{IN\ max}$	Max Input Signal	THD = 0.3%	2	2.5		V_{RMS}
$I_{N\ S}$	Input Separation (1)		80	100		dB
VOLUME CONTROL						
C_{RANGE}	Control Range			17.625		dB
A_{VMIN}	Min. Attenuation		-0.5	0	0.5	dB
A_{VMAX}	Max. Attenuation		16.7	17.625	18.6	dB
A_{STEP}	Step Resolution		0.175	0.375	0.575	dB
E_A	Attenuation Set Error		-1		1	dB
E_T	Tracking Error				0.5	dB
V_{DC}	DC Steps	adjacent attenuation steps		0	3	mV
GRAPHIC EQUALIZER						
THD	Distortion			0.01	0.1	%
C_s	Channel Separation		80	100		dB
e_{NO}	Output Noise	BW = 20Hz to 20KHz flat, AV = 0dB		8	20	μV
		A curve		6		μV
		BW = 20Hz to 20KHz AV = 0dB All bands = max. boost All bands = max. cut		 24 6		 μV μV
S/N	Signal to Noise Ratio	A_V = 0dB; V_{ref} = $1V_{RMS}$		100		dB
B_{step}	Step Resolution		1	2	3	dB
C_{RANGE}	Control Range	max boost/cut	±12	±14	±16	dB
VDC	DC Steps	Adiacent Control Steps		0.5	3	mV
AUDIO OUTPUTS						
V_O	Output Voltage	THD = 0.3%	2	2.5		V_{RMS}
R_L	Output Load Resistance		2			KΩ
C_L	Output Load Capacitance				10	nF
R_O	Output Resistance		5	10	20	Ω
V_{OUT}	DC Voltage Level		4.2	4.5	4.8	V
BUS INPUTS						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
I_{IN}	Input Current		-5		+5	μA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA			0.4	V
ADDRESS PIN (Internal 50KΩ pull down resistor)						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		V_{CC} -1V			V

NOTE: The input is grounded thru the 2.2μP capacitors

DEVICE DESCRIPTION

The TDA7317 is a five bands, digitally controlled stereo Graphic Equalizer.
The device is intended for high quality audio application in Hi-Fi, TV and car radio systems where feature like low noise and THD are key factors. A mixed Bipolar Cmos Technology allows:
Cmos analog switches for pop free commutations, high frequency op.amp. (GWB = 10MHz) and high linearity polisilicon resistor for THD = 0.01 (at Vin = 1Vrms) and a S/N ratio of 102dB.
The internal Block Diagram is shown on page 1.

The first stage is a volume control. The control range is 0 to -17.625dB with 0.375dBstep.
The very high resolution (0.375dB step) allows the implementation of closed loop amplitude control system completely free from any acustical effect (stepping variation and pumping effect).

The volume control is followed by a serial five bands equalizer. Each filtering cell is the biquad cell shown in fig. 1

The internal resistor string is fixing the boost/cut value while the buffer makes the Q (quality factor) and central frequency, set by external components, fully indipendent from the internal resistors. Each filtering cell is realized using only 4 external components (2 capacitors and 2 resistors) allowing a flexible selection of centre frequency fo, Q factor and gain. Here below the basic formulae and the key features of each band pass filter are reported:

f_o = center frequency

Gv = gain/loss at the center frequency f_o
Gv = 20log(Av)

$$Q = \frac{f_o}{f_2 - f_1}$$

where f_2, f_1 = 3dB Bandwidth limits.

$$A_v = \frac{(R2 \cdot C2) + (R2 \cdot C1) + (R1 \cdot C1)}{(R2 \cdot C1) + (R2 \cdot C2)}$$

$$Q = \frac{\sqrt{(R1 \cdot C1 \cdot R2 \cdot C2)}}{(R2 \cdot C1) + (R2 \cdot C2)}$$

$$f_o = \frac{1}{2\pi \cdot \sqrt{(R1 \cdot R2 \cdot C1 \cdot C2)}}$$

If C1 is fixed, then:

$$C2 = \frac{Q^2}{A_v - 1 - Q^2} \cdot C1$$

$$R2 = \frac{1}{2\pi \cdot C1 \cdot f_o \cdot \frac{(A_v - 1) \cdot Q}{(A_v - 1 - Q^2)}}$$

$$R1 = \frac{(A_v - 1)^2}{A_v - 1 - Q^2} \cdot R2$$

Likewise, the components'values can be determined by fixing one of the other three parameters. Referring to fig. 1 the suggested R2 value should be higher than 2KΩ in order to have a good THD (internal op. amp. current limit).
Viceversa the R1 value should be equal or lower than 51KΩ in order to keep the "click"(DC step) very low.

A typical application is shown by fig. 2

Fig. 1

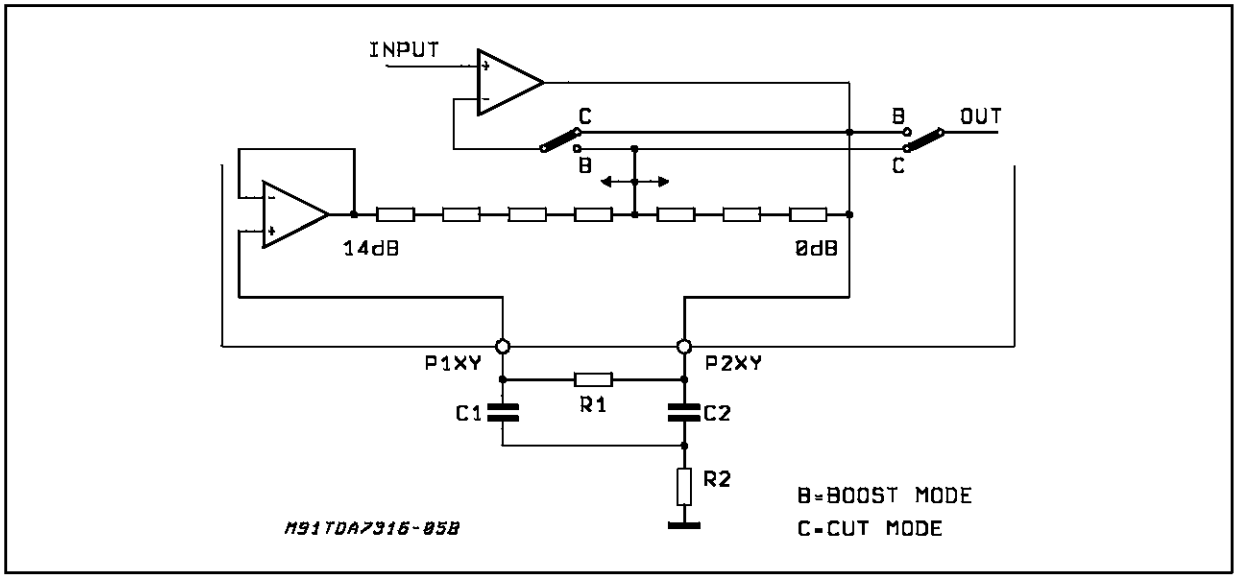
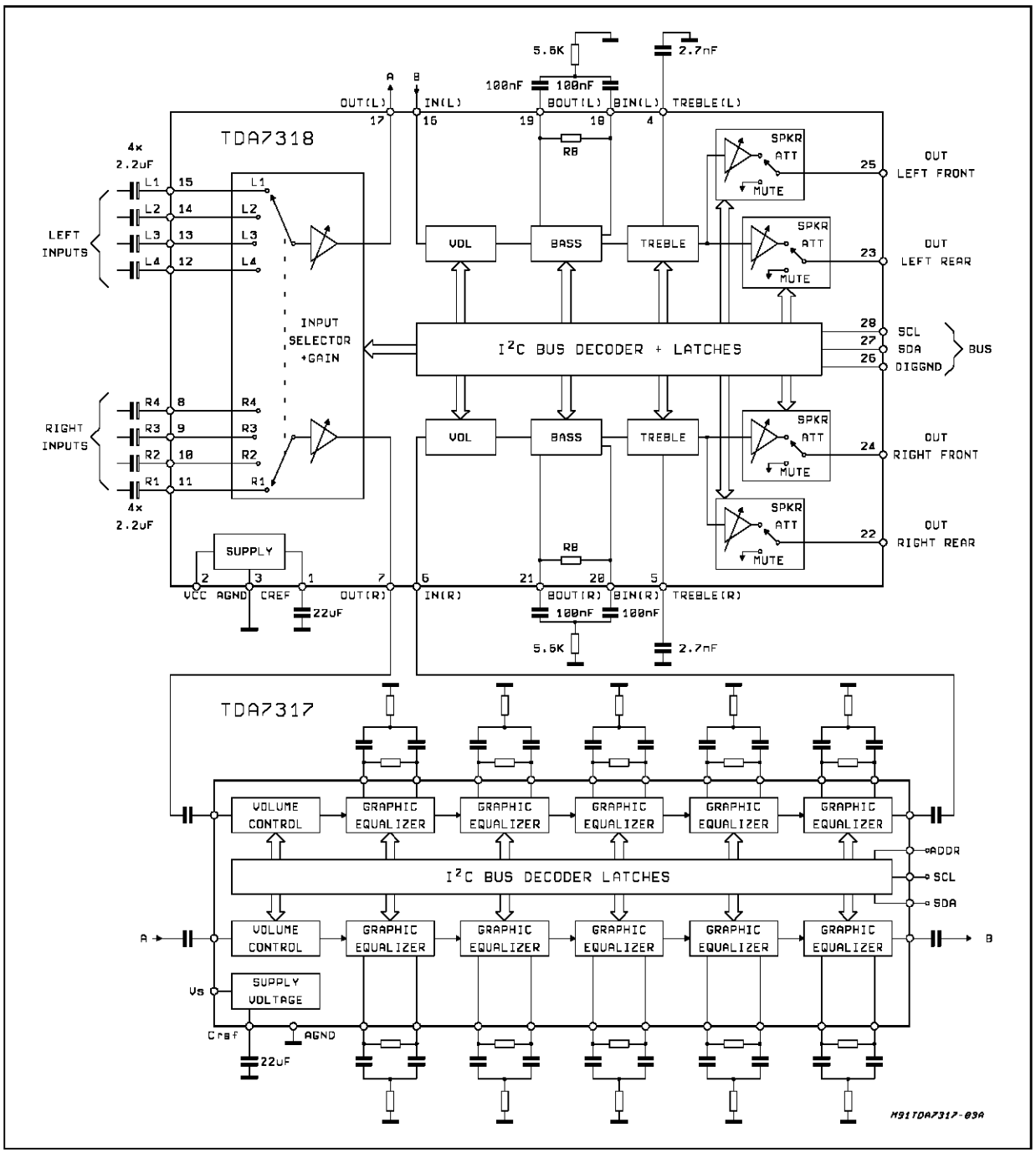


Figure 2: Application Circuit



The five bands graphic equalizer is used in conjunction with a TDA7318 (or another audioprocessor of the SGS-THOMSON 731X family).

The audioprocessor bass and treble tone can furnish two extra filter bands.

Application requiring higher number of external equalizer bands could be implemented by cascading 2 or more TDA7317 devices. In fact the dedicated ADDR pin allows 2 addresses selection. Anyway, the address of the graphic equalizer is different from the audioprocessor one.

For example 11 bands are implemented by use of 2 TDA7317 plus an audioprocessor (TDA731X family).

In case one filtering cell is not needed, a short circuit must be provided between the P1xy and P2xy pins.

I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7317 and viceversa takes place thru the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

Data Validity

As shown in fig. 3, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown in fig.4 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte Format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 5). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simplier transmission: simply it generates the 9th clock pulse without checking the slave acknowledging, and then sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

Figure 3: Data Validity on the I²CBUS

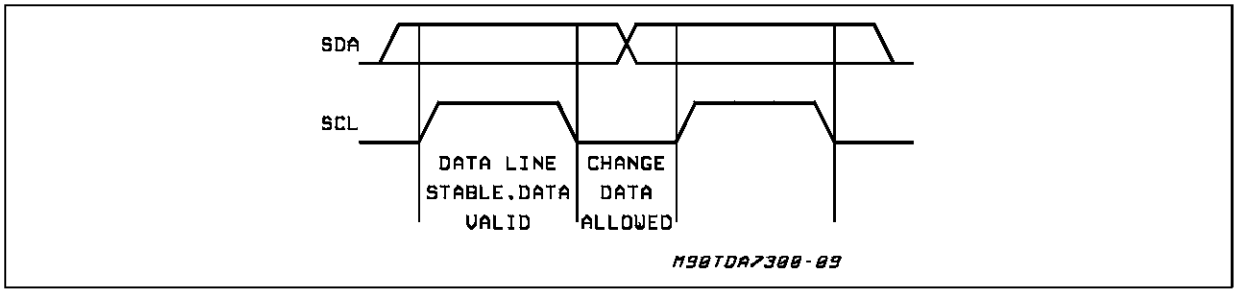


Figure 4: Timing Diagram of I²CBUS

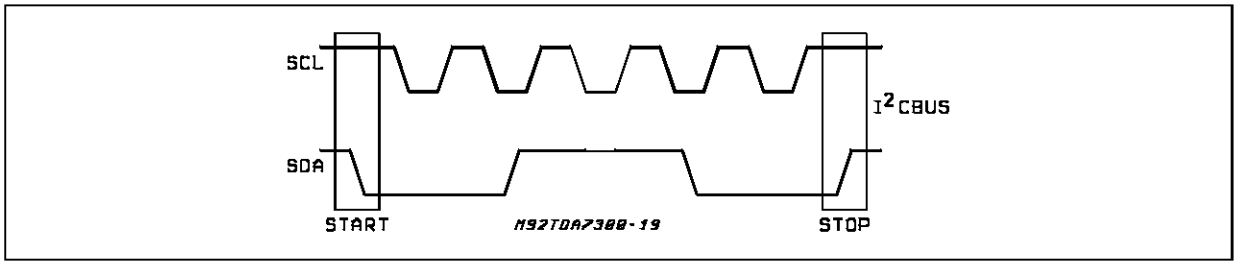
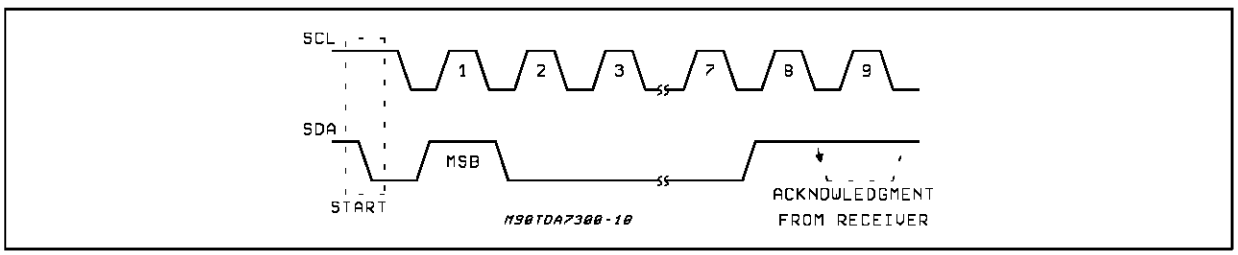


Figure 5: Acknowledge on the I²CBUS

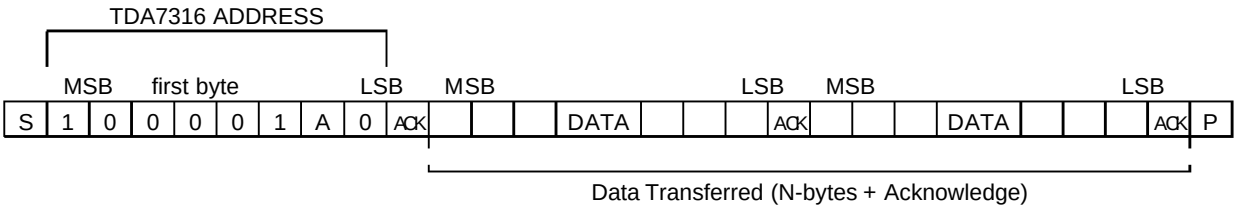


SOFTWARE SPECIFICATION

Interface Protocol

The interface protocol comprises:

- A start condition (s)
- A chip address byte, containing the TDA7317 address (the 8th bit of the byte must be 0). The TDA7317 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge
S = Start
P = Stop

MAX CLOCK SPEED 100kbits/s

SOFTWARE SPECIFICATION

Chip address (84 or 86 Hex)

1 MSB	0	0	0	0	1	A	0 LSB

A = Logic level on pin ADDR

A = 1 if ADDR pin = open

A = 0 if ADDR pin = connected to ground

SOFTWARE SPECIFICATION (continued)

DATA BYTES (detailed description)

Volume

MSB							LSB	FUNCTION
0	X	B2	B1	B0	A2	A1	A0	Volume 0.375dB steps
					0	0	0	0
					0	0	1	-0.375
					0	1	0	-0.75
					0	1	1	-1.125
					1	0	0	-1.5
					1	0	1	-1.875
					1	1	0	-2.25
					1	1	1	-2.625
0	X	B2	B1	B0	A2	A1	A0	Volume -3dB steps
		0	0	0				0
		0	0	1				-3
		0	1	0				-6
		0	1	1				-9
		1	0	0				-12
		1	0	1				-15

Graphic Equalizer

MSB							LSB	FUNCTION
1	D3	D2	D1	D0	S2	C1	C0	
	0	0	0					Band 1
	0	0	1					Band 2
	0	1	0					Band 3
	0	1	1					Band 4
	1	0	0					Band 5
	D3	D2	D1	1	C2	C1	C0	cut
	D3	D2	D1	0	C2	C1	C0	Boost
					0	0	0	0dB
					0	0	1	2dB
					0	1	0	4dB
					0	1	1	6dB
					1	0	0	8dB
					1	0	1	10dB
					1	1	0	12dB
					1	1	1	14dB

AX = 0.375dB steps, BX = 3dB steps, CX = 2dB steps, X = dont'care

STATUS AFTER POWER-ON RESET	
Volume	-17.25dB
Graphic equalizer bands	-12dB

APPLICATION INFORMATION

A typical application is indicated in figure 4, while the P.C. Board and components layout are reported in figure 5. The external components, are calculated for 2 different max boost/cut conditions

TABLE 1: Max Boost/cut = 20 dB (each cell = ±14dB)

	F (HZ)	Q	R1 (KΩ)	R2 (KΩ)	C1 (nF)	C2 (nF)	Av max (dB)
BAND 1	10363.38	1.49	47	5.1	0.820	1.2	13.52
BAND 2	261.03	1.49	47	5.1	33	47	13.63
BAND 3	1036.34	1.49	47	5.1	8.2	12	13.52
BAND 4	3168.08	1.49	47	5.1	2.7	3.9	13.57
BAND 5	59.75	1.11	43	7.5	220	100	13.88

For THD performance the sequence Band 1, 2, 3, 4, 5, is recommended

TABLE2: Max Boost/cut = 17dB (each cell = ±12dB)

	F (HZ)	Q	R1 (KΩ)	R2 (KΩ)	C1 (nF)	C2 (nF)	Av max (dB)
BAND 1	10158.00	1.15	33	6.2	1.2	1	11.83
BAND 2	250.81	1.21	30	5.1	47	56	11.33
BAND 3	977.34	1.20	39	6.8	10	10	11.75
BAND 4	3429.00	1.25	39	6.2	2.7	3.3	11.67
BAND 5	61.82	1.15	33	6.2	180	180	11.27

Figure 4

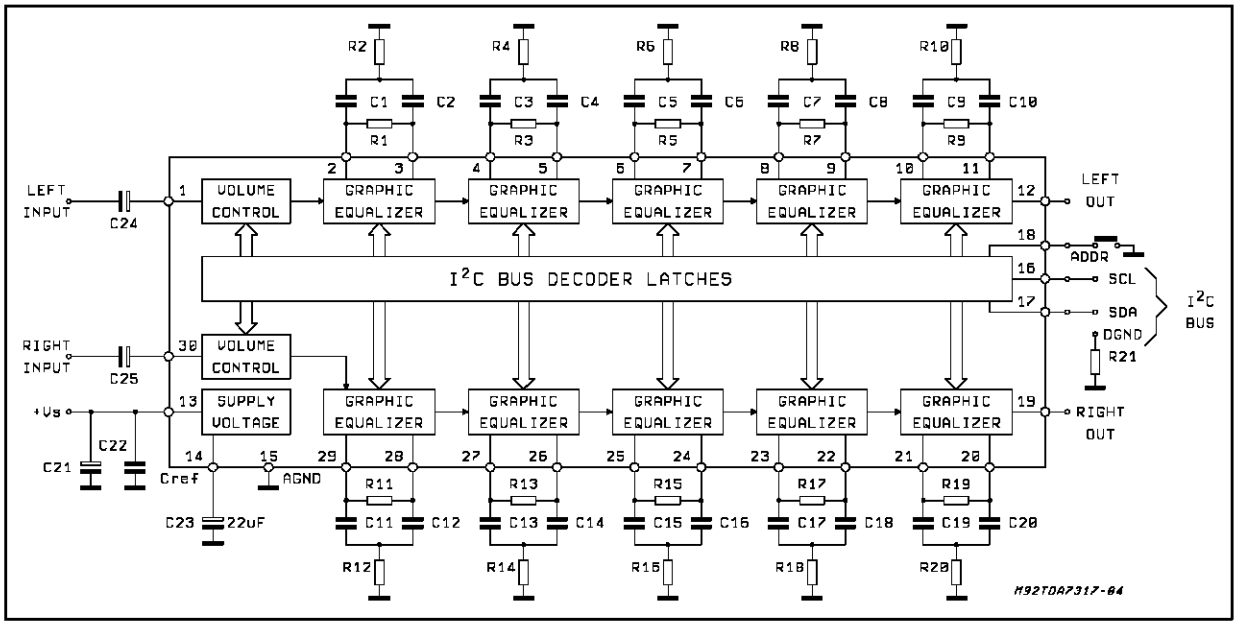
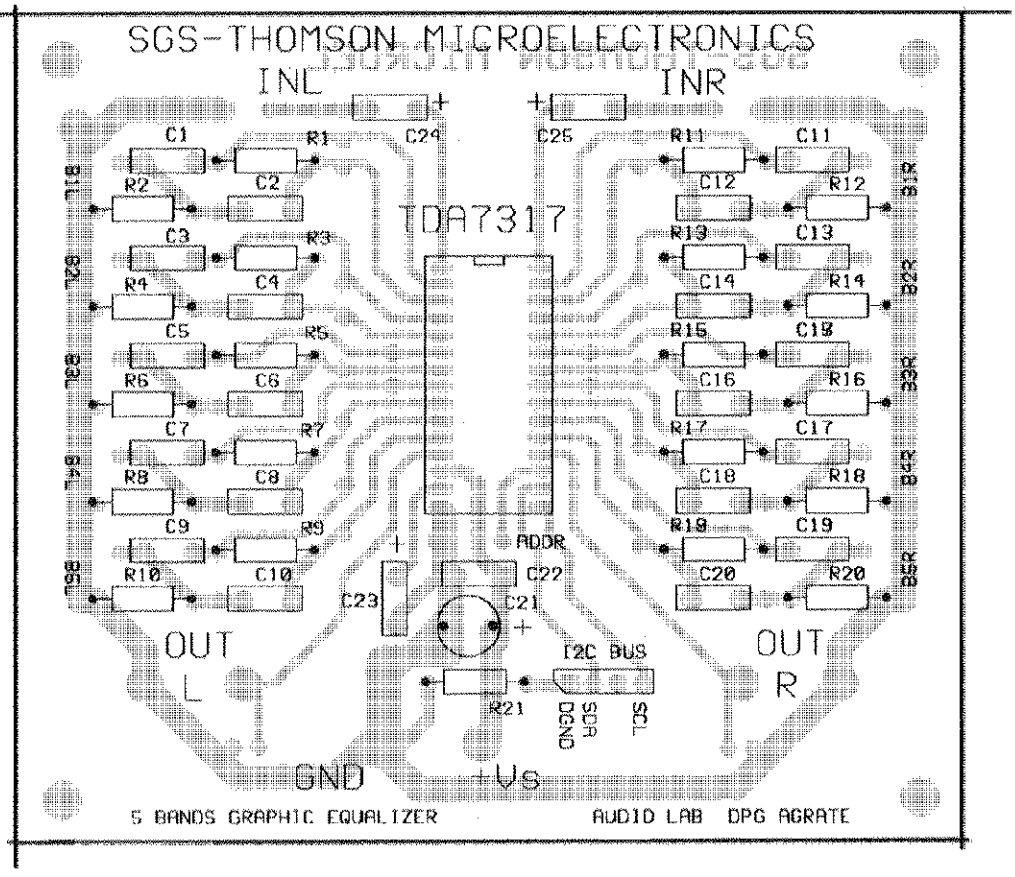


Figure 5: PCP Board and components layout of the figure 4 (scale 1:1)



Measurements done on the test jig of fig. 5 using the components indicated in table2, are reported in figg. 6, 7,8.

Figure 6: Frequency Response

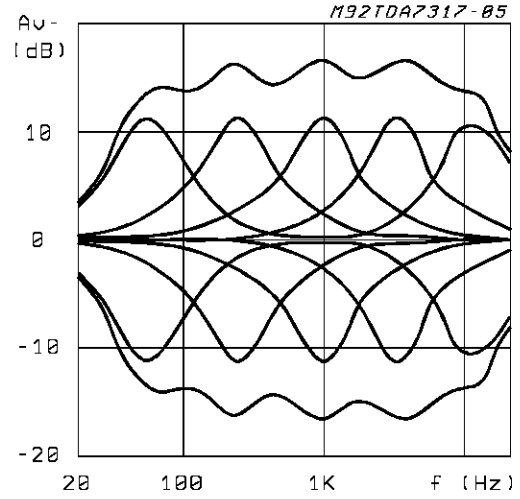


Figure 7 THD vs Frequency Max Boost/cut = ±14dB

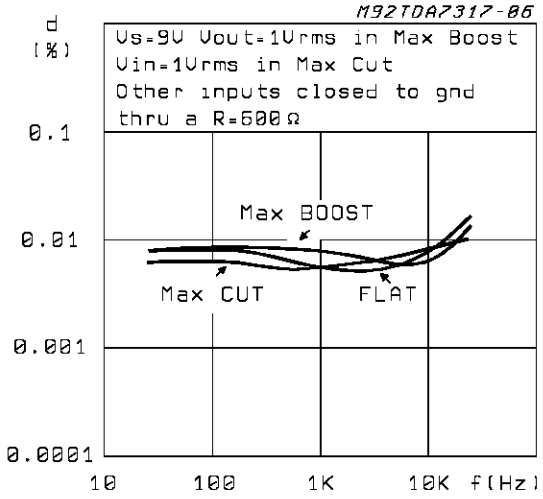
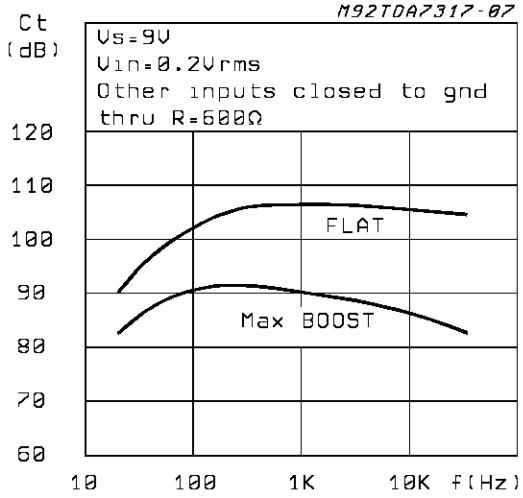


Figure 8: Cross Talk vs Frequency



SDIP30 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.12	0.15	0.18
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	0.76	0.99	1.40	0.030	0.039	0.055
C	0.20	0.25	0.36	0.008	0.01	0.014
D	27.43	27.94	28.45	1.08	1.10	1.12
E	10.16	10.41	11.05	0.400	0.410	0.435
E1	8.38	8.64	9.40	0.330	0.340	0.370
e		1.778			0.070	
e1		10.16			0.400	
L	2.54	3.30	3.81	0.10	0.13	0.15
M	0°(min.), 15°(max.)					
S	0.31			0.012